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DESIGN AND DEVELOPMENT OF CPLD BASED TEMPERATURE MEASUREMENT AND CONTROL SYSTEM

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ABSTRACT

This paper deals with the design and development of CPLD based VLSI system to measure and control the temperature. The RTD (resistance temperature detector) Pt100 is used as a temperature sensor, and is interfaced with the CPLD (XC9572) manufactured by Xilinx. The output that is produced by the sensor needs to be converted into quantized voltage levels in order to send it as an input to an ADC. This can be achieved by a signal conditioning circuit built in the laboratory using LM324. The necessary code is written in the hardware description language VHDL. ISE (Integrated Simulation Environment) version 9.1i suite is used for software development which is one of the EDA (Electronic Design Automation) tool offered by the Xilinx Company.

KEYWORDS: CPLD, ISE9.1i, ADC, RTD Pt100, LCD, Relay

INTRODUCTION

Today, almost every VLSI design team applies programmable logic devices to facilitate the overall design process and to minimize the final cost. Fast reconfigurable logic together with high rate ADC (analog-to-digital converter) opens this area for digital data processing and control [1]. The design performed here uses Xilinx CPLD (XC9572) , JTAG for Boundary scan mode, Temperature sensor (RTD Pt100), Low Power Quad Operational Amplifier(LM324), ADC(AD574), Auto Ranging 4 ½ Digital Multimeter (SM5011A) and a 2-lines/16-characters LCD (liquid crystal display), Electromagnetic Relay.

Temperature sensors play a pivotal role in many measurements and other integrated microsystems. Different types of sensors like, RTD, thermocouples, thermistors, thermostats, solid state sensors, IC sensors etc., are used in different applications [2]. Temperature is one of the most measured physical parameters. Thermocouple and RTD sensors are adequate for most high-temperature measurements, but one should choose a sensor that has characteristics best suited for the application. RTDs offer high precision and an operating range of -200°C to +850°C. They also have an electrical output that is easily transmitted, switched, displayed, recorded, and processed using suitable data-processing equipment. Because RTD resistance is proportional to temperature, applying a known current through the resistance produces an output voltage that increases with temperature. Knowledge of the exact relationship between resistance and temperature allows calculation of a given temperature. The change in electrical resistance vs. temperature of a material is termed as the "temperature coefficient of resistance" for that material. Moreover, an RTD is the most stable, accurate, and linear device available for temperature measurement [3]. The resistivity of metal used in an RTD (including platinum, copper, and nickel) depends on the range of temperature measurements desired. The nominal resistance of a platinum RTD is 100Ω at 0°C.

BLOCK DIAGRAM

The block diagram of the hardware developed in the present work is shown in Figure 1.

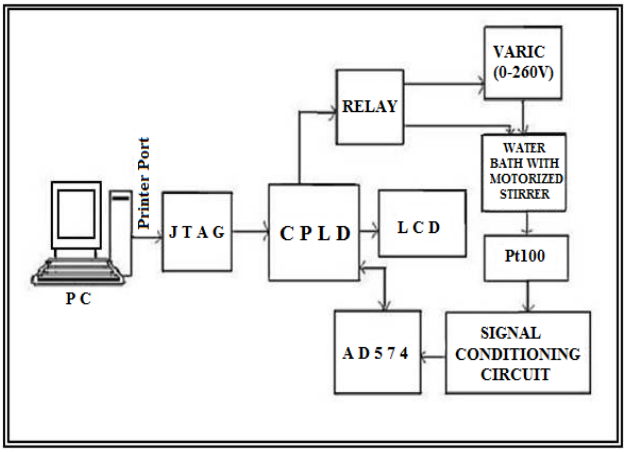

Figure 1: Block Diagram of CPLD Based Temperature Measurement and Control System

DESCRIPTION OF THE HARDWARE DETAILS

Water Bath with Motorized Stirrer

The Photograph of the water bath with motorized stirrer is shown in Figure 2. The water bath contains a vessel with $3/4^{th}$ of water, Stirrer and a heating element. The vessel is kept in a wooden box and the top is also closed with insulating cap. A small 'L' shaped iron rod is attached to the DC motor shaft, which acts as stirrer. The DC motor is fixed on the top of the wooden box. Here the stirrer is used for getting the uniform temperature in the water bath. The Pt100 sensor and probes of the digital thermometer are also dipped in the bath through the holes beside the DC motor on the top of the wooden box. When power is ON, DC motor gets energized to rotate along with the stirrer is also rotated to get the uniform temperature throughout the experiment.

Figure 2: Waterbath with Motorized Stirrer

Temperature Sensor and Signal Conditioning Circuit

RTD Pt100 in the form of wire wound design is used as a temperature sensor, because it gives values of better accuracy, linearity and long-term stability. A two-wire lead resistance compensating technique is adopted in using the Pt100. In order to obtain the exact temperature, it is of paramount importance to avoid self heating of the sensor, which means that the current passing through the sensor should be held low. The voltage drop across the Pt 100 is in the order of micro or mill volt. This voltage is amplified suitably using the linearizing and signal conditioning circuit developed in the laboratory as shown in Figure 3.

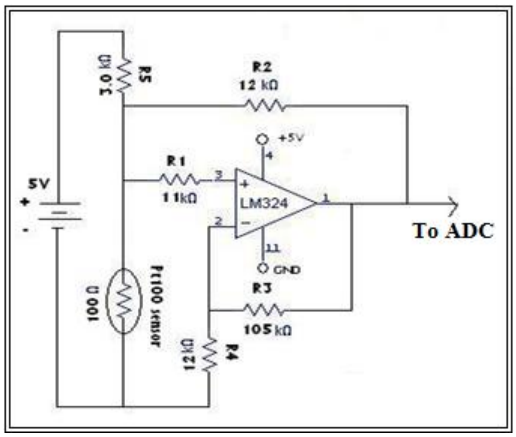

Figure 3: Signal Conditioning Circuit

Analog to Digital Converter

Most of the physical quantities vary continuously, which is the characteristic of the analog world. Such a continuously varying quantity has to be invariably quantized in to digital format. This process calls for a module that converts the analog quantity in to its equivalent digital value. This is accomplished using ADC. The ADC used in the present work is AD574, which works on the principle of "**successive-approximation technique"**. The AD574 is a complete 12-bit successive-approximation analog to digital converter [4]. A high precision voltage reference and clock are included on-chip, and the circuit gives full rated performance without external circuitry or lock signals.

Features of AD574

- The AD574 interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
- The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 volts to +10 volts and 0 volts to +20 volts unipolar; –5 volts to +5 volts and –10 volts to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15 ppm/°C typical T.C. The reference is available externally and can drive up to 1.5 mA beyond the requirements of the reference and bipolar offset resistors.

CPLD (Complex Programmable Logic Device)

CPLD is a combination of a fully programmable AND/OR array and a bank of macrocells [5]. The AND/OR array is reprogrammable and can perform a multitude of logic functions. Macrocells are functional blocks that perform combinatorial or sequential logic, and also have the added flexibility for true or complement, along with varied feedback paths. CPLD is a programmable logic device with complexity between that of PALs and FPGAs, and architectural features of both. The building block of a CPLD is the macrocell, which contains logic implementing disjunctive normal form expressions and more specialized logic operations. CPLD's predictable timing characteristics make them ideal for critical, high-performance control applications [6]. Typically, CPLDs have a shorter and more predictable delay than FPGAs and other programmable logic devices. Because they are inexpensive and require relatively small amounts of power, CPLDs are often used in cost-effective, battery-operated portable applications.

The target CPLD device used in the present work is XC9572 manufactured by Xilinx. Design development and debugging is carried on a low-cost, full-featured kit provided by ADM (Applied Digital Microsystems) Pvt., Ltd., Mumbai. This board provides all the tools required to quickly begin design and verifying CPLD platform designs. Designs are based on 10 MHz clock. The board includes a 1x16 pin connector, which can be used to connect a standard 5V character LCD module. LCD module can display 2 lines of 16 characters is made up of 5x8 Pixel.

Details of XC9572

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration [7]. It is comprised of eight 36V18 Function blocks, providing 1,600 usable gates with propagation delays of 7.5ns. Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation

GENERATING PROGRAMMING FILE

JEDEC Files

JEDEC files are XC9572 CPLD programming files generated by the Xilinx fitter [8]. They are ASCII text files containing programming information and, optionally, functional test vectors that can be used to verify the correct functional behavior of the programmed device. One JEDEC file is required for each XC9572 device in the JTAG programming chain as shown in Figure 4. The name of the JEDEC file is called as <design name>.jed

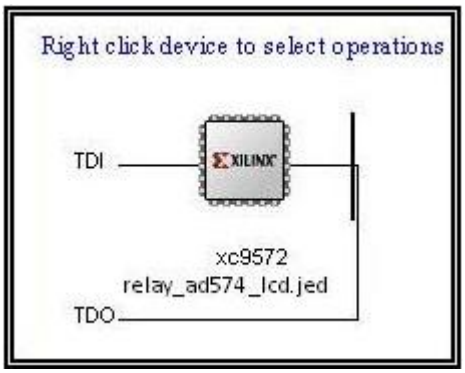

Figure 4: JTAG Chain which Shows the Configured Device

Device Configuration

The device is configured after generating a programming file. To verify the performance of the temperature measurement and control system, the JEDEC file i.e., *.jed file is downloaded into the target XC9572.

TEMPERATURE MEASUREMENT AND CONTROL BY INTERFACING RTD TO CPLD USING AD574

Figure 5 shows the schematic of CPLD based temperature measurement and control system and Figure 6 shows its photograph. RTD is inserted in the water bath; when the temperature of the water bath changes, then the resistance of RTD is also changes. The output produced by the RTD needs to be converted into quantized voltage levels. This can be achieved through a process known as “signal conditioning”.

The signal conditioning circuit gives the analog voltage, which is proportional to the temperature. The signal conditioning may be a current to voltage conversion or simply amplification. The output of the signal conditioning circuit is fed to the ADC (AD574), since FPGA can process only digital data. AD574 converts the input analog voltage into 12-bit digital data.

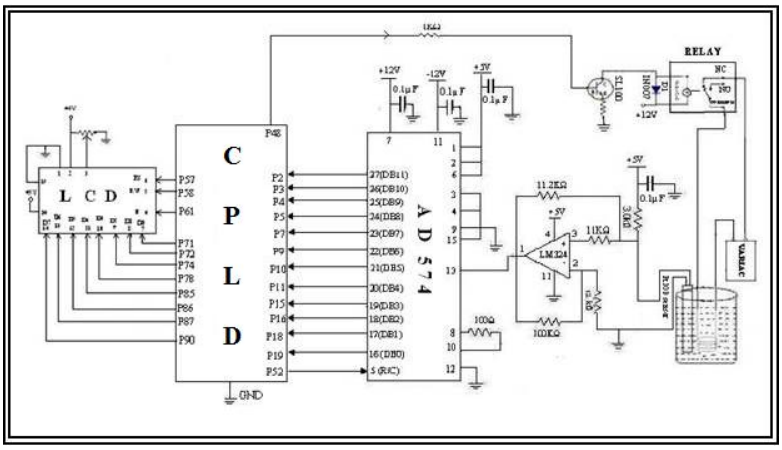

Figure 5: Schematic of CPLD Based Temperature Measurement and Control System

Figure 7 shows the graph drawn between temperature and digital output, which is a linear curve. Look- up table was developed using this curve. In order to initiate AD574, CPLD sends a high signal to R/$\overline{C}$ pin of AD574. The conversion starts when signal to R/$\overline{C}$ goes low. When the end of conversion signal of the AD574 is found to be high, it is an indication to the CPLD that 12-bit data which represents the temperature can be read in. CPLD compares the corresponding temperature value from look-up table and finally displays on LCD. The result is displayed in two lines as shown in Figure 8. The first line displays TEMPERATURE: and the second line displays the measured temperature value with first decimal and units as °C.

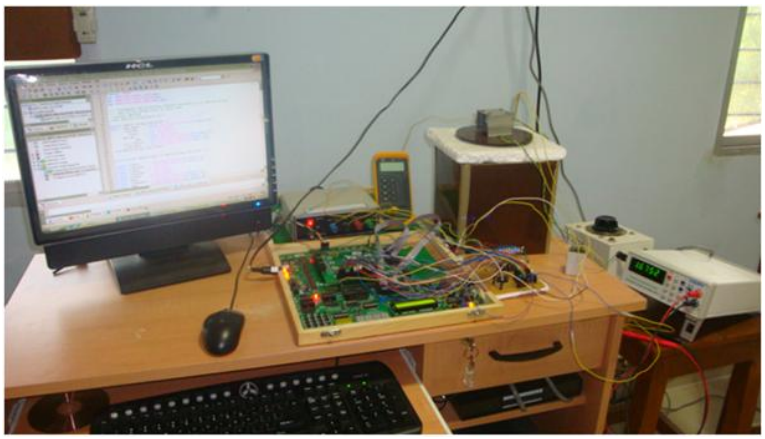

Figure 6: Photograph of the CPLD Based Temperature Measurement and Control System

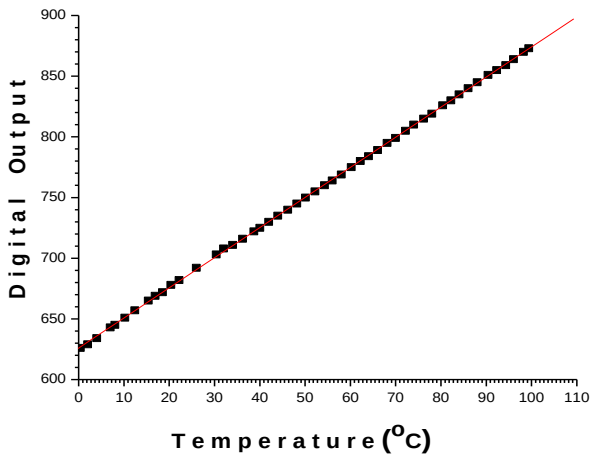

Figure 7: Temperature Vs. Digital Output

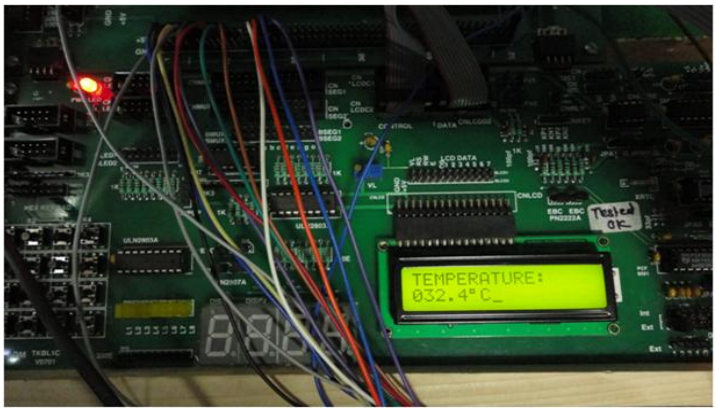

Figure 8: Photograph Showing Results on LCD

INTERFACING ELECTROMECHANICAL RELAY WITH CPLD

To control the power delivered to the heater, the Electro Mechanical Relay is used. With this relay, we can control a 240V AC powered immersion heater. To change the position of relay contact, a constant voltage should be applied across the relay coil. NPN transistor SL100 is used to control the relay with 12V coil, operating from +12V supply as shown in Figure 9. A Series base resistor R2 is used to set the base current for SL100, so that the transistor is driven into saturation when the relay is to be energised. That way, the transistor will have minimal voltage drop, and hence delivering most of the 12V to the relay coil. Initially when the coil is not energized, there will be a connection between the common terminal and normally closed (NC) pin. But when the coil is energized, this connection breaks and a new connection between the common terminal and normally open (NO) pin will be established. A diode (IN4007) is connected across the relay coil, to protect the transistor from damage due to the back emf pulse generated in the relay coil's inductance, when SL100 turns off. That is, when the voltage is removed from the coil, it needs some path to discharge the stored energy in it. So the diode (IN4007) creates that path until the coil discharges [9].

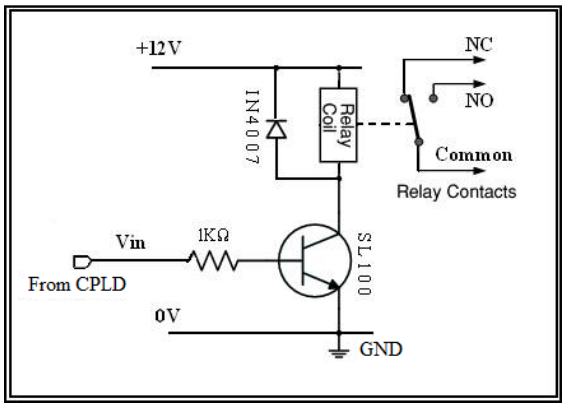

Figure 9: Electromechanical Relay Interfacing Circuit

The transistor on the input of the relay supplies the drive for the relay, isolates the CPLD from the relay and holds the relay in the NC position when the power is turned ON. The displayed temperature is compared by the CPLD with the set-point temperature. If it is less than the desired value, then CPLD sends a LOW signal to the relay interfacing circuit, so that the relay remains in the NC position. Hence the power is supplied continuously to the heater and the temperature increases [10]. If the desired temperature is reached, then CPLD sends a HIGH signal to the interfacing circuit, so that the relay contact shifts to NO position, which disconnects power supply to the heater. Thus the temperature is maintained at steady state and controls at a desired value. The photograph of the signal conditioning circuit, ADC and Relay unit is shown in Figure 10.

Flow Chart

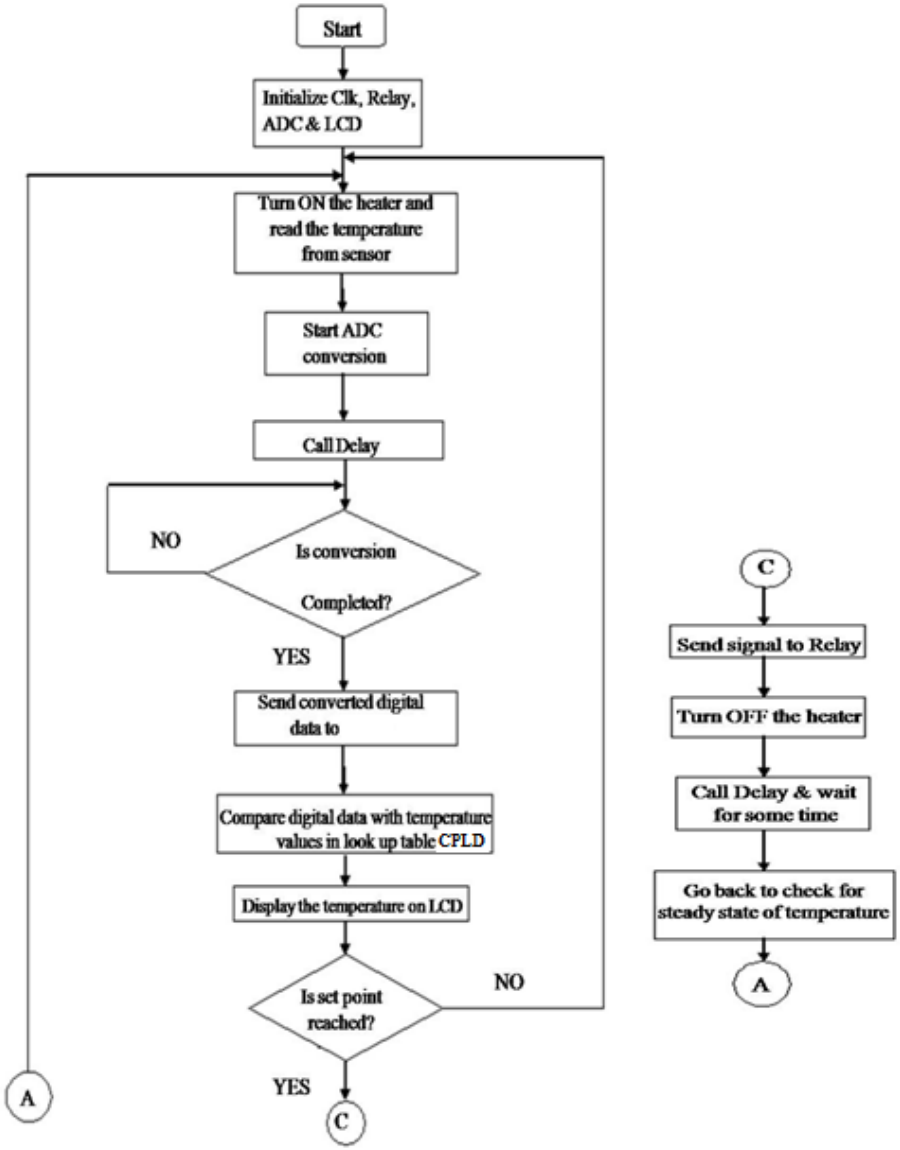

Figure 10: Flow Chart of the VHDL Program Developed in the Present Work

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